

EN0-001 Q&As

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QUESTION 1

in a	Cortex-A9	processor,	CP14	system	control	l registers	are used	d f	or:
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- A. Cache control operations
- B. Address translation operations
- C. Debug control and status information
- D. Architecture feature ID registers

Correct Answer: C

QUESTION 2

In which type of storage will the compiler preferentially place frequently accessed variables?

- A. Stack
- B. Heap
- C. Registers
- D. Hard disk

Correct Answer: C

QUESTION 3

An Advanced SIMD intrinsic has the prototype:

uint8xl6x2_t vld2q_u8 (uint8_t const * ptr);

How many bytes does this intrinsic load from memory?

- A. 2
- B. 16
- C. 32
- D. 256

Correct Answer: C

QUESTION 4

Which of the following is preserved in dormant mode?



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- A. Core register contents
- B. CP15 (system) register settings
- C. Debug state
- D. Cache contents

Correct Answer: D

QUESTION 5

Which of the following functions can be performed by a spinlock?

- A. Encrypting sensitive data on a network
- B. Preventing interrupts from being received by a CPU
- C. Preventing unauthorized access to an ARM powered device
- D. Protecting a critical section or data structure from concurrent access

Correct Answer: D

QUESTION 6

Literal pool loads to access constants at run-time can be minimized by:

- A. Ensuring constants can be encoded as immediates in the current instruction set.
- B. Storing the code in ROM.
- C. Using Thumb code rather than ARM code.
- D. Compiling and linking as position-independent code.

Correct Answer: A

QUESTION 7

A deeply embedded real-time industrial control system is missing some hard real-time interrupt deadlines. Which of the following performance analysis techniques is the most suitable for identifying which routines are causing the problem?

- A. Use an ETM instruction trace profiler, which outputs information about the program as it runs
- B. Add some serial logging to the software, which outputs information about the program as it runs
- C. Add a new interrupt handler, which is triggered off a timer, and dump information about the interrupted process
- D. Use a JTAG sample-based profiler, which periodically halts the CPU, and dumps information about the interrupted process

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Correct Answer: A	

QUESTION 8

In a single-processor system, which of these operations requires a barrier instruction to guarantee correct operation?

- A. Copying data from Flash to RAM
- B. Changing from one privileged mode to another
- C. Loading code into memory and then executing it
- D. Incrementing a RAM location that will be read by an interrupt handler

Correct Answer: C

QUESTION 9

In an ARMv7 processor that includes the Advanced SIMD (NEON) extension, how many single precision floating point values can be stored in the Q0 register?

- A. 1
- B. 2
- C. 4
- D. 8

Correct Answer: C

QUESTION 10

Which of the following options lists the power modes in order of increasing overhead of entry and exit from run mode?

- A. Shutdown, dormant, standby
- B. Dormant, standby, shutdown
- C. Shutdown, standby, dormant
- D. Standby, dormant shutdown

Correct Answer: D

QUESTION 11

When linking with the standard C library, which library functions MUST be redefined in order to port your code to a new piece of production hardware?

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- A. Functions that are not compliant with the ISO C library standard
- B. Functions that are not compliant with the 1985 IEEE 754 standard for binary floating-point arithmetic
- C. Target-dependent functions which use semihosting
- D. Functions called implicitly by the compiler

Correct Answer: C

QUESTION 12

What is an "Entry point" in an application?

- A. A place where execution can start
- B. The location of the main () function
- C. The lowest address contained in a program image
- D. A location where the linker can store additional information

Correct Answer: A

QUESTION 13

The ARMv7-A virtual memory management system supports 32-bit (short) and 64-bit (long) page table descriptors. The sizes of a small page in a short descriptor and a small page in a long descriptor are:

- A. 1 KB and 4KB respectively
- B. 4KB and 4KB respectively
- C. 4KB and 16KB respectively
- D. 16KB and 16KB respectively

Correct Answer: B

QUESTION 14

The Performance Monitoring Unit (PMU) of a Cortex-A9 processor permits direct measurement of which one of the following?

- A. Cache Size
- B. Clock Speed
- C. Program size
- D. Numbers of instructions executed



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Correct Answer: D

QUESTION 15

Which instruction would be used to return from a Reset exception?

- A. MOVS PC, R14
- B. MOVSPC, R13
- C. Architecturally not defined
- D. SUBS PC, R14, #4

Correct Answer: C

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